

Listing of Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

- 1 **1.** (Currently amended) A system, comprising:
 - 2 at least a first jitter buffer store having a plurality of first jitter buffer
 - 3 entries arranged into groups that each store data for a particular data channel,
 - 4 the first jitter buffer entries being accessible by first jitter buffer addresses;
 - 5 at least a first valid bit store having a plurality of valid buffer entries,
 - 6 each valid buffer entry having a plurality of bit locations that indicate the
 - 7 status of at least one entry from multiple groups of the first jitter buffer, the
 - 8 valid buffer entries being accessible by valid bit store addresses; and
 - 9 an address generator that receives at least a first portion of first jitter
 - 10 buffer addresses to generate corresponding valid bit store addresses.

- 1 **2.** (original) The system of claim 1, wherein:
 - 2 the address generator generates bit mask values for valid bit store
 - 3 entries from at least a second portion of the first jitter buffer addresses.

- 1 **3.** (original) The system of claim 1, wherein:
 - 2 the address generator adds a valid bit store base address to the at least
 - 3 first portion of first jitter buffer addresses.

- 1 **4.** (original) The system of claim 1, further including:
2 the at least first jitter buffer store is formed in a first memory device;
3 and
4 the at least first valid bit store is formed in a second memory device.
- 1 **5.** (original) The system of claim 4, wherein:
2 the first memory device comprises a static random access memory
3 (SRAM).
- 1 **6.** (original) The system of claim 1, wherein:
2 the at least first jitter buffer store includes a plurality of jitter buffer
3 stores, each jitter buffer store including entry groups of different sizes.
- 1 **7.** (original) The system of claim 6, wherein:
2 the plurality of jitter buffer stores includes the first jitter buffer store
3 having entry groups that store X amount of data of a data channel, a second
4 jitter buffer store having entry groups that store at least 2X amount of data of
5 a data channel.
- 1 **8.** (original) The system of claim 1, further including:
2 a time stamp counter that provides a time stamp value that is
3 incremented; and
4 jitter buffer entries for data channels are periodically read from the at
5 least first jitter buffer according to the time stamp value.
- 1 **9.** (original) The system of claim 1, further including:
2 a processor that reads at least a portion of the data from first jitter
3 buffer entries and writes the at least portion of the data to a local buffer, the
4 processor resetting the value of at least one bit in a corresponding valid buffer
5 entry when all of a first jitter buffer entry is written to the local buffer.

- 1 **10.** (original) The system of claim 9, wherein:
2 each first jitter buffer entry includes N portions, and the processor
3 reads each entry N times before resetting the value of the bit in the
4 corresponding valid buffer entry.
- 1 **11.** (original) A system for storing data from multiple channels received from an
2 asynchronous network and outputting such data to a synchronous network,
3 comprising:
4 a jitter buffer arranged into a plurality of jitter buffer groups that each
5 include M entries, where M is a real number, each jitter buffer group storing
6 data for a different data channel;
7 a valid buffer having a plurality of valid buffer entry groups, each
8 valid buffer entry including status bits corresponding to at least one of the M
9 entries in N different jitter buffer groups; and
10 an address translator that translates a jitter buffer entry address for a
11 jitter buffer entry into the valid buffer entry address having the status bit for
12 that entry.
- 1 **12.** (original) The system of claim 11, wherein:
2 each jitter buffer group comprises M consecutive addressable entries
3 of a semiconductor memory device.
- 1 **13.** (original) The system of claim 12, wherein:
2 the jitter buffer and valid buffer are formed in two different memory
3 devices.
- 1 **14.** (original) The system of claim 12, wherein:
2 each valid buffer entry corresponds to one particular entry in each of
3 the N jitter buffer entry groups.
- 1 **15.** (original) The system of claim 12, wherein:

2 the address translator includes
3 a base address store that stores a base address for the jitter
4 buffer,
5 a separator for separating a jitter buffer address into at least a
6 first portion and a second portion, and
7 an adder for adding the base address and the first portion of the
8 jitter buffer address.

1 16. (original) The system of claim 15, wherein:
2 one status bit in a valid buffer entry is selectable by masking the valid
3 buffer entry according to the second portion of the jitter buffer address.

1 17. (Currently amended) A method for receiving data from an asynchronous network and
2 outputting such data to a synchronous network, comprising the steps of:
3 providing a jitter buffer having a plurality of entries for storing data;
4 providing a valid memory having a plurality of entries for storing
5 status bits for each jitter buffer entry;
6 receiving data for multiple channels;
7 storing data segments for each channel in a corresponding group of
8 jitter buffer entries;
9 setting a status bit in the valid memory entry to a valid state when data
10 is written to the corresponding jitter buffer entry, swizzling the write address
11 to generate the corresponding jitter buffer entry;
12 reading data from jitter buffer entry; and
13 setting the status bit of a valid buffer entry to an invalid state when
14 data is read from the corresponding jitter buffer entry, swizzling the
15 read address to generate the corresponding jitter buffer entry.

1 18. (original) The system of claim 17, wherein:
2 receiving data includes receiving data packets having multiplexed

3 data.

1 19. (currently amended) The system of claim 17, wherein:

2 reading data segments includes reading data segments from a jitter
3 buffer read address that includes at least a portion of a time stamp value that
4 increments; and

5 ~~—setting a status bit in a valid buffer entry includes swizzling the read~~
6 ~~address to generate the corresponding jitter buffer entry.~~

1 20. (currently amended) The system of claim 17, wherein:

2 storing data segments includes writing data segments to a jitter buffer
3 write address that includes at least a portion of a time stamp value that
4 increments; and

5 ~~—setting a status bit in a valid buffer entry includes swizzling the write~~
6 ~~address to generate the corresponding jitter buffer entry.~~